

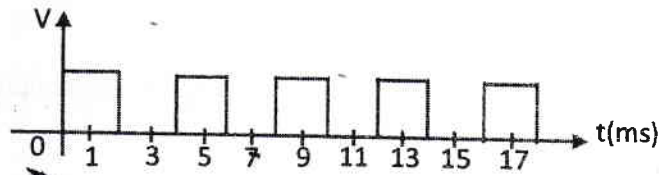
Bago University
Department of Physics
Second Semester Examination, September 2019

Fourth Year (BSc)
(Physics Specialization)

Phys 4102
Electronics
Time Allowed: (3) Hours

Answer any Six questions.

- 1 (a) Define rise time, fall time and pulse width for a pulse.
 (b) What is the duty cycle? Is the pulse waveform in figure periodic or non-periodic? Determine the duty cycle of the waveform in figure.



- 2 (a) Convert the decimal number 105_{10} into (i) binary, (ii) octal and (iii) hexadecimal.
 (b) Find the decimal equivalents of (i) 10110_2 , (ii) 35_8 and (iii) $5A_{16}$.
 (c) Convert the number 11010011_2 into (i) octal and (ii) hexadecimal.
- 3 (a) Convert the following numbers into binary number.
 (i) 105_8 (ii) $3FD_{16}$ (iii) 53_8
 (b) Convert the decimal numbers 72 and 27 into (i) binary, (ii) octal and (iii) hexadecimal numbers.
- 4 (a) Express the logic symbol, logic expression, truth table and operation of given logic gates.
 (i) 2-input NAND gate (ii) 3-input OR gate
 (b) The waveforms of inputs A and B are shown below.
 (i) Draw the waveform of X if $X = A.B$.
 (ii) Draw the waveform of Y if $Y = \overline{A + B}$.



- 5 (a) What are the twelve basic rules of Boolean algebra?
 Prove $B + BC = B$ and $(B + C)(B + D) = B + CD$.
 (b) Using Boolean algebra techniques simplify the following expression.
 $X(Y + Z) + Y(Y + Z) + XY$
- 6 (a) State DeMorgan's first and second theorems. Describe the rules of Boolean algebra.
 (b) Map the following SOP expressions on a Karnaugh map.
 (i) $\overline{A} + \overline{A}\overline{B} + A\overline{B}\overline{C}$
 (ii) $\overline{A}\overline{B}CD + \overline{A}B\overline{C}D + A\overline{B}\overline{C}D + ABCD + A\overline{B}C\overline{D} + \overline{A}B\overline{C}D + A\overline{B}C\overline{D}$

- 7 (a) Implement a simplified logic circuit for the following truth table.

INPUT			OUTPUT
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

- (b) Draw the logic circuits for the following equations. Simplify the equations and draw the simplified logic circuits.
- (i) $Y = AB + BC + ABC$
- (ii) $Z = ABC + CD + CDE$
- 8 (a) Express the logic diagram, logic symbol and truth table of a gated S-R latch.
- (b) A 555 timer is configured to run in the astable mode using $R_1 = 2.2 \text{ k}\Omega$, $R_2 = 4.7 \text{ k}\Omega$ and $C_1 = 22 \text{ nF}$. Find (i) the time the output is High, (ii) the time the output is Low, (iii) time period, (iv) frequency of the output and (v) duty cycle of the output.
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